

D4.3

Preliminary Energy harvesting system with regulated 3.3 V output based on μ -plasma systems

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Abstract

This deliverable deals with the development of plasma switches to optimise the energy management of triboelectric generators (TENGs), whose high AC-voltage output must be rectified and converted into low DC-voltage in a Buck architecture. We first fabricated plasma switches in silicon, operating up to 800 V. They have proven their effectiveness but also show degradation due to intense discharges, in particular for voltages above 400 V. To remedy this, we then focused on silicon carbide (SiC), a wide bandgap material capable of withstanding much higher electric fields and temperatures, preventing local melting and ensuring greater robustness. Three technological approaches (SiC/Si bonding, PECVD deposits and all-SiC structures) are envisaged. Preliminary results with the SiC/Si bonding process are shown.

Keywords

Plasma switch, DC-DC conversion, Micro-technologies, Silicon Carbide

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Abbreviations

SEM	Scanning Electron Microscope
TENG	TriboElectric NanoGenerator
PMS	Power Management System
DC	Direct Current
SOI	Silicon on Insulator
(D)RIE	(Deep) Reactive Ion Etching
WBG	Wide Bandgap
SiC	Silicon Carbide
GaN	Gallium Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

Executive summary

This deliverable focuses on the design of plasma switches based on MEMS technologies for managing energy from triboelectric generators (TEGs). TEGs produce alternating current (AC) energy that must be converted to direct current (DC) in order to power electronic devices. The associated power management system (PMS) has two stages: (i) a first rectification stage, which accumulates the charge in a capacitor at an optimal voltage in order to maximise the power harvested, then (ii) a Buck DC-DC down conversion stage, which adapts this often very high voltage (several hundred volts) to the practical needs of the applications (1–5 V). For maximizing the energy conversion, the Buck converter needs a high-voltage and floating switch.

For this switching, plasma switches appear to be an effective solution, particularly when the output voltage of the TEGs exceeds 300 V after rectification. The ON/OFF actuations of plasma switches are self-controlled by design, following the Paschen law, and then do not need complex and power consuming electronic. During the ON actuation, an electrostatic discharge occurs between two closely spaced electrodes as long as the voltage across the anode and the cathode of the switch exceeds the Paschen limit.

During the GRAPHERGIA project a first generation of plasma switches in silicon operating up to 800 V was fabricated. Experiments confirmed the expected triggering, but also revealed structural damage linked to intense discharge currents, causing local melting of the silicon. To overcome these limitations, silicon carbide (SiC) plasma switches were studied. This wide bandgap semiconductor can withstand electric fields ten times higher than silicon and extreme temperatures, which prevents the micro-melting previously observed. Three manufacturing processes were explored: SiC bonded to silicon, PECVD deposition of SiC on Si, and all-SiC structures (the most promising but costly). SiC is a very new material for MEMS devices and new processes need to be developed in order to fabricate plasma switches in SiC. The initial results validated the direct Si/SiC assembly and paved the way for future developments, in particular the optimisation of thicknesses and etching steps.

In conclusion, the work lays the foundations for robust plasma switches for TEGs' power management systems, with a gradual transition from silicon to SiC, which is more suited to high voltages and harsh environments.



1 Introduction

This deliverable concerns STO-4 and focuses on the design of plasma switches using MEMS technologies. The plasma switch is a key component of the energy management circuits dedicated to TENGs, which are detailed in Deliverable D4.1.

The output from a triboelectric nanogenerator (TENG) is alternating-current (AC) energy, which requires rectifiers to convert it to direct-current (DC) energy suitable for powering electronic devices. A good Power Management System (PMS) for any kinetic energy harvester must maximize the amount of energy delivered to an electrical load in a minimum amount of time. For electrostatic transducers such as TENGs, the PMS must first dynamically bias the TENG with its optimum DC voltage, knowing that the converted power is proportional to the square of this voltage. This is the objective of the first stage of the conditioning circuit, which rectifies the TENG output signal into a DC voltage.

Depending on the situation, the harvested charges are transferred directly to an electrical load or to a second stage to reduce and stabilize the output voltage. Therefore, a PMS for TENGs typically has two stages: a first stage to maximize the harvested energy by maintaining a high DC voltage across the TENG, and a second to shape the output signal to an appropriate voltage for the targeted application. Such PMS is shown in **Figure 1**.

1.1 The first stage: signal rectification

The first step in a typical TENG PMS is to generate a DC voltage from the TENG's AC output signal. For most TENGs, this is achieved through the use of charge-pump circuits which will progressively accumulate the electrical charges generated by the TENG with each mechanical cycle in a (relatively) large capacitor (referred to as C_{rect} in the following) at the rectifier output.

As the number of mechanical actuation cycles increases, the voltage across C_{rect} gradually reaches a constant saturation voltage in case the rectifier is a stable charge-pump, or increases exponentially until a defect appears (high losses in diodes and/or capacitors, electrostatic spark in the transducer...) in case the rectifier is an unstable charge-pump. In both cases there is an optimum voltage that will maximize the harvested power while keeping the system safe.

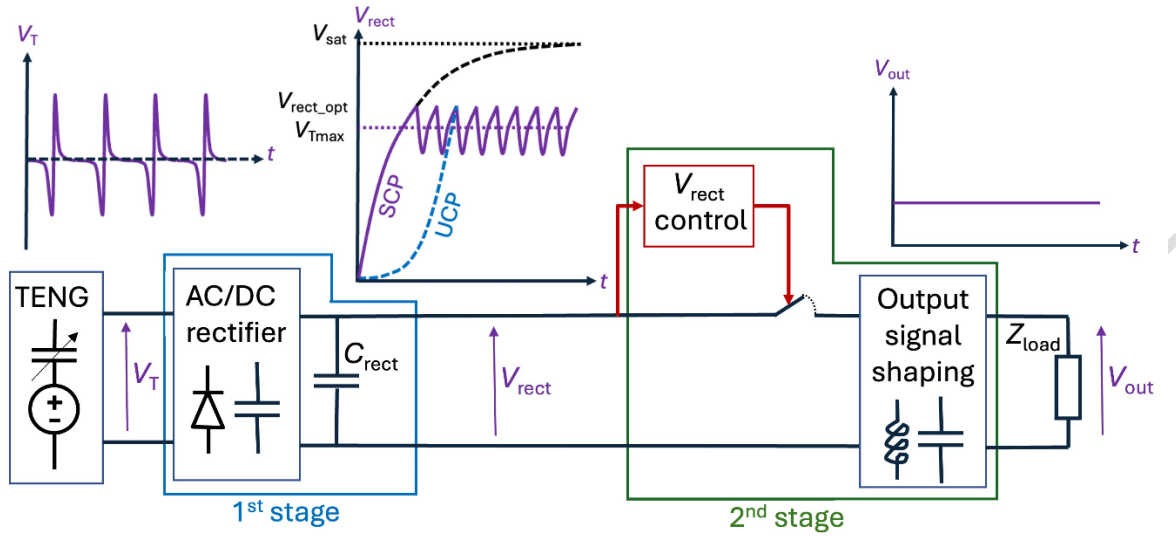


Figure 1. Ideal power management system for TENG. The 1st stage reaches the optimum conversion point, the 2nd stage maintains the maximum power operation and generates the expected output signal 0.

Therefore, one of the objectives of the 2-stage PMS is to maintain the rectifier output close to this optimum voltage. This is possible if a switch is activated to extract the accumulated energy in C_{rect} (or a part of it) when the rectifier output voltage is around its optimum. The switch actuation mechanism can be of several types: electronic [2], electrostatic [3] or mechanical [4].

1.2 The second stage: shaping the output DC signal

With state-of-art tribo-electret layers and/or with the use of unstable charge-pumps, the optimum output voltage of a rectifier for TENGs can be very high. If this helps to maximize the harvested power, most applications need a regulated low voltage between 1 and 5 volts. In this case, a second stage acting as a DC-DC voltage converter must be used, possibly followed by a voltage regulator. If the first stage accumulates the collected charges in C_{rect} , the second stage transfers part of these charges to a larger capacitor through an inductor, activating a floating switch at a frequency much lower than the mechanical frequency [5]. This circuit is like a Buck DC-DC converter, except that the switch is only activated when the targeted voltage across C_{rect} is reached. The second stage of the PMS therefore has two roles: (i) to optimise power conversion efficiency by maintaining a high/optimal DC bias voltage across the TENG, and (ii) to adjust the PMS output voltage V_{store} to the value required by the system to be powered.

2 Silicon-based plasma switch

2.1 First run

If the expected actuation voltage is less than ~ 300 V, the switch must be electronically controlled, preferably with a dedicated CMOS IC to minimize interference and additional power consumption. For higher voltages, a plasma switch consisting of two conductors separated by a few microns can be used. When V_{rect} exceeds the limit defined by Paschen's law, an electrostatic discharge occurs between the two electrodes of the switch, transferring charges from V_{rect} to the next stage. If one of the switch electrodes is mobile, using MEMS technology for example, very narrow hysteresis can even be achieved without the need for controlled electronics [6]. This minimum voltage of 300 V may seem very high, but with unstable charge-pumps, it can be easily reached even with poor quality tribo-electret layer, but at the cost of a long charging time.

Figure 2 shows an example of a plasma switch made of bulk silicon fabricated at UGE prior to the GRAPHERGIA project and working between 300 and 400 volts. The TENG used for the experiment is a 6×6 cm² conductive PU foam contacting a PTFE layer.

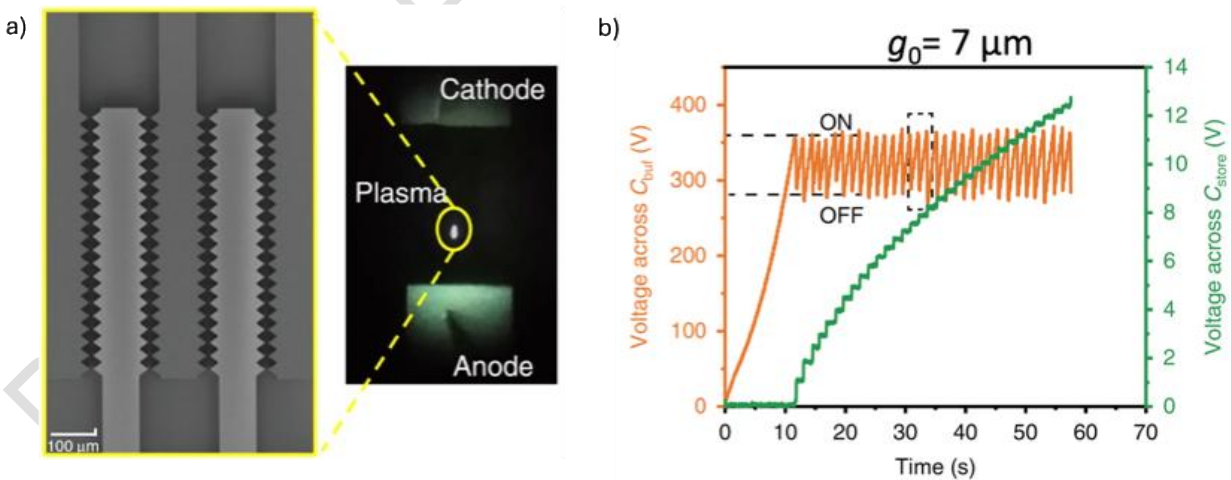


Figure 2. a) SEM image of a plasma switch made of 40 μm -thick bulk silicon, photo of the micro-plasma, b) measure of the voltage across at the output of the rectifier (C_{buf}) and at the output of the Buck DC-DC down converter (C_{store}) [6].

2.1 Second run

Since the harvested power increases with the square of the optimum voltage at the output of the rectifier, we designed new plasma switches supposedly working up to 800 V, with the objective to gain a factor 4 of the energy conversion. A new lithography mask has been designed with four types of designs for plasma switches with only fixed electrodes. Each dice contains switches of different types. The first design has a single rectangular structure (a finger) from the anode leading to the cathode. The ends of both are flat, making it a plate-to-plate geometry. The second design that is positioned on the same dice has a slight variation: at the strip at which the anode and cathode are the closest, an array of triangle-like intrusions has been added to both sides. The third design has 3 fingers attached to the anode and two at the cathode. This design provides significantly more area for the discharge to occur. Analogously to the previous dice, the second sample on this dice contains a modified design with extrusions. These four designs have been used as a base to create variations with 7, 9 or 12 μm gap between the anode and the cathode.

Figure 3 shows a schematic of the two dices and the 4 designs.

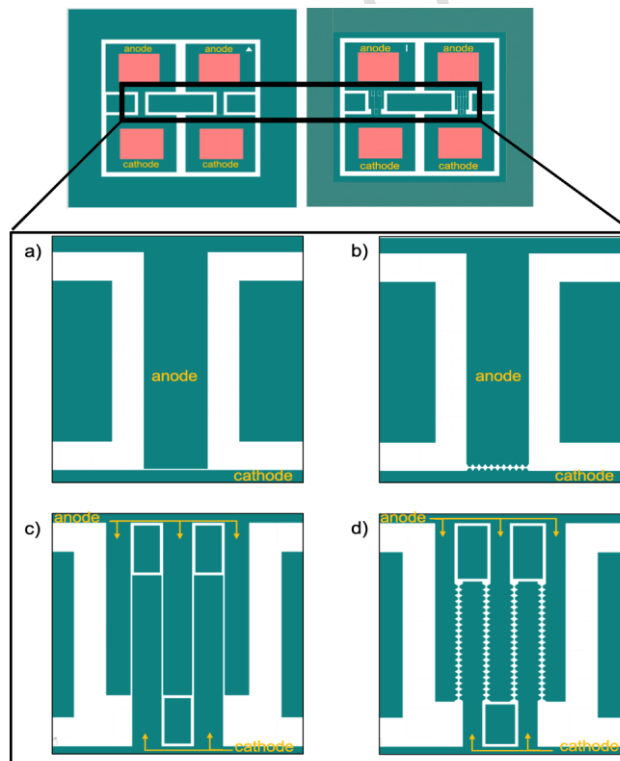


Figure 3. Schematic of the two dices, each containing two plasma switches. a) Switch made of a single beam with a flat surface facing the cathode. b) Switch made of a single beam with 10 triangle-like

extrusions at its end facing the same extrusions on the cathode. c) Comb-like structure of five fingers d,) Similar comb-like structure with 100 extrusions distributed over the 3 anode and the 2 cathode fingers.

The devices were fabricated in the clean room at UGE/ESIEE Paris in a silicon-on-insulator (SOI) wafer having a 40 μm -thick device layer, a 2 μm box layer and a 400 μm thick handle layer. The fabrication process starts by growing a 0.8 μm oxidation layer on top of the SOI, followed by the deposition of a photoresist for photolithography and the etching of the oxide layer. That is done so that the trenches between the anode and the cathode, as the openings for pads, can be obtained. To form the connection pads, a 0.8 μm layer of aluminum is deposited, followed by a photolithography and an etching step. After the aluminum is etched, the 40 μm of the device layer of the SOI are etched using deep reactive ion etching (DRIE). The final step consists in the oxide etching using vapor HF. Before samples are ready to use, the aluminum is annealed and samples are diced. The process is presented in **Figure 4**.

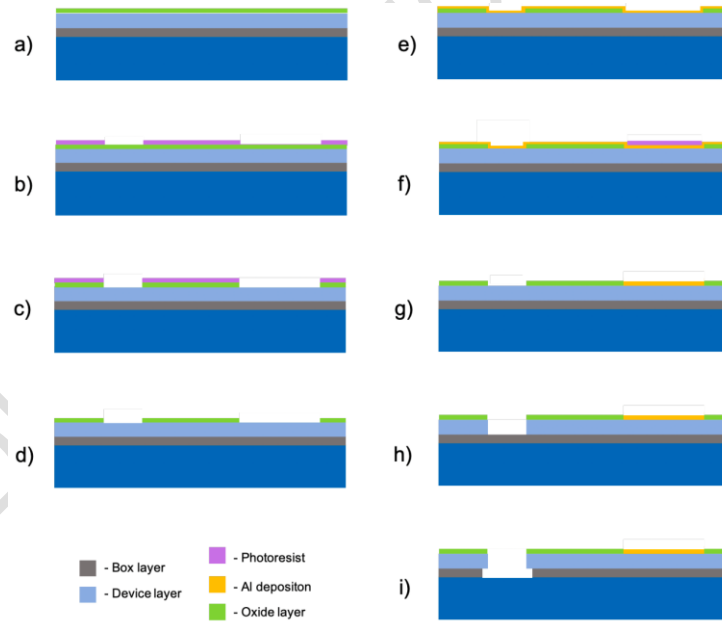


Figure 4. The fabrication process of plasma switches on a SOI wafer. a) SOI wafer with oxidation. b) Photolithography. c) RIE silicon dioxide. d) Resist removal. e) Aluminum deposition. f) Photolithography. g) Aluminum etching and resist removal. h) DRIE of silicon. i) Oxide etching (vapor HF).

2.2 Testing of plasma switches

The plasma switch of this second run was tested with a 10x10 TENG mounted on a linear motor. The setup is shown in **Figure 5**. First, switches with the smallest gap of 7 μm were tested with a half-wave rectifier. The theoretical actuation value of switch obtained from the Pashen law is 369 V. The voltage signal before the switch was monitored using an electrometer and the signal from the capacitor after the switch is fed through an operational amplifier (OPA) in a follower configuration so that the output signal can be observed on an oscilloscope. For both outputs, capacitive voltage dividers were used. The circuit and measurement results on three different samples are shown in **Figure 6**.

The curve in red corresponds to the output of the half-wave rectifier and the one in black represents the voltage over the capacitor after the plasma switch. The switch actuation voltage is first around 350 V which is close to the expected value. By magnifying the segment of the graph at which the switch conducts, it has been measured that it is active for 0.6 ms, which is not enough to discharge the input capacitor of the electrometer. This explained why the curved doesn't restart at zero after each switch actuation.

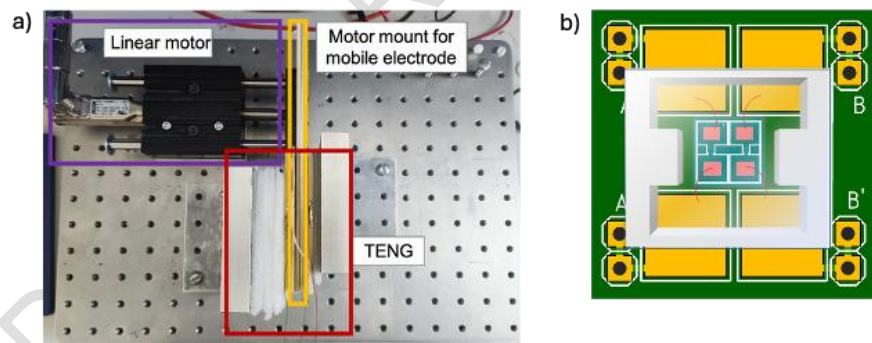


Figure 5. a) Setup used for testing the second run of plasma switches. b) Packaging used for the switches: wire bonding on a PCB, 3D printing spacer and protection glass.

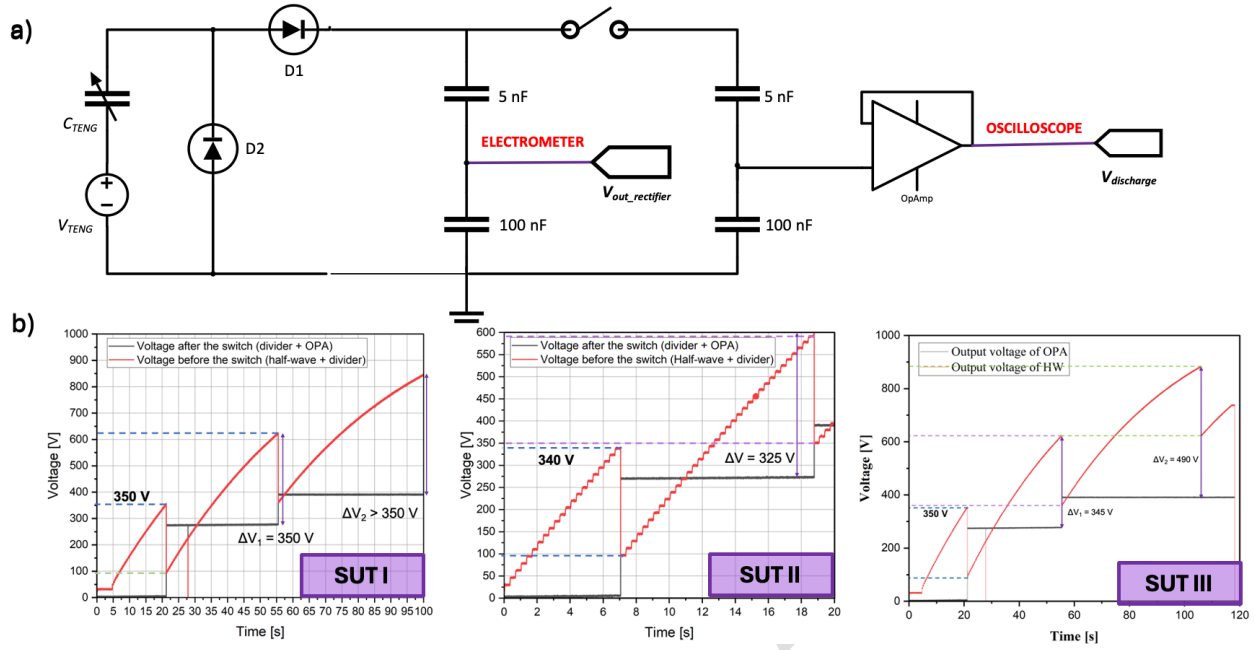


Figure 6. a) Schematic of the circuit used for the initial test. b) Results for 3 plasma switches with a gap of $7 \mu\text{m}$.

Figure 6 shows that the output signal varies significantly from the second or third actuation, showing some changes in the structure. This is confirmed with optical microscope and SEM images of the samples after actuation as shown in **Figure 7**. It is assumed that the current generated during the discharge is of such a high intensity that it is large enough to fuse the silicon and so modifying the gap between the anode and the cathode of the switch.

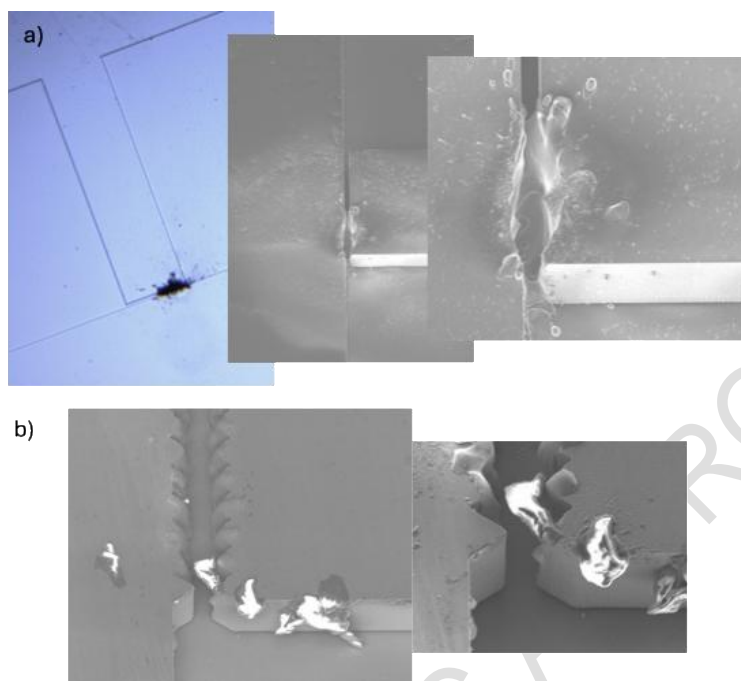


Figure 7. a) Optical and SEM images of two plasma switches in silicon after several actuations.

3 Plasma switch in SiC

In SiC material, higher local electric fields than in silicon can be developed and higher local temperatures can be withstood. We anticipate that, unlike silicon structures, electrical breakdown in high-voltage SiC plasma switches will not generate micro-melting in small areas inside or on the surface of semiconductor crystals. Indeed, SiC is a wide bandgap semiconductor (WBG) material which, compared to silicon, has superior physical properties for electronic components or sensors intended for harsh environments. SiC has already begun to replace silicon on an industrial scale in power electronic components used today in electric vehicles, a rapidly growing market.

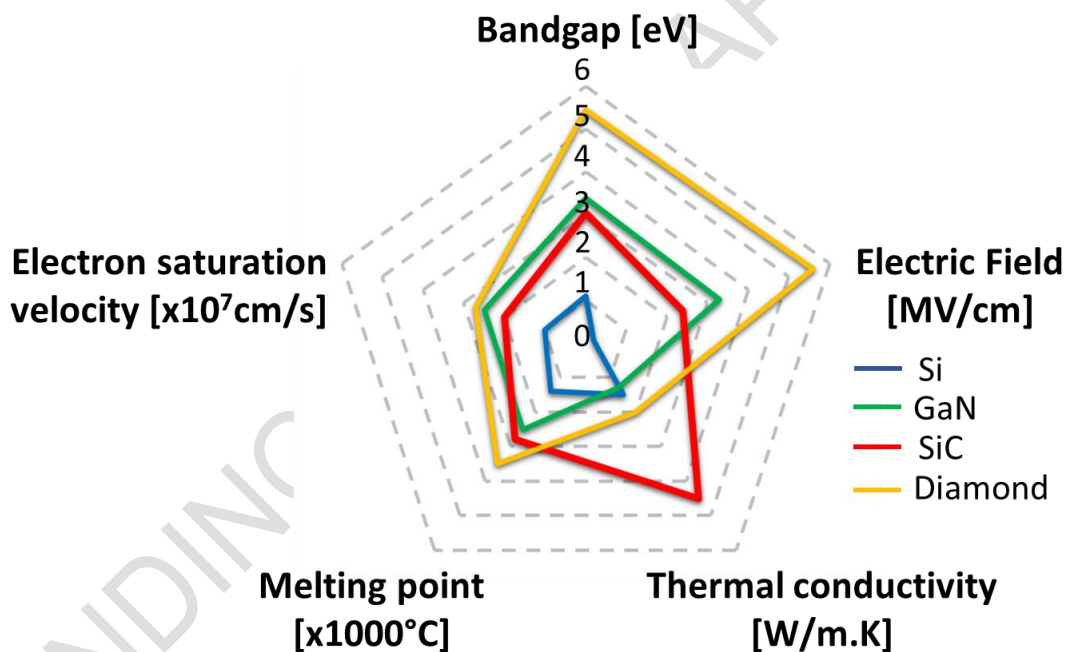


Figure 8. SiC physical properties compared to silicon and other WBG semiconductor materials

SiC can withstand electric fields ten times higher than silicon and temperatures several times higher before thermal runaway of junctions or crystal deterioration (cf. **Figure 8**). Compared to other WBG materials such as GaN or diamond, SiC is superior in terms of technological maturity, with MOSFET switches developed on large, high-quality wafers (up to 200 nm).

During the first year of GRAPHERGIA project, we developed a new 100 to 150 mm SiC technology line with all the necessary steps for manufacturing SiC devices, including doping, plasma etching, passivation, specific metallisation for ohmic contacts, etc., and we considered several processes for the fabrication of plasma-switches in SiC.

3.1 Plasma switches with SiC layers

3 processes are considered for the fabrication of plasma-switches in SiC:

- the bonding SiC/Si structure (**Figure 9**),
- the PECVD SiC/Si structure (**Figure 10**),
- the all SiC structure (**Figure 11**).

3.1.1 Bonding SiC/Si structure

Advantages:

- High doped SiC layers can be obtained
- With known doping from the SiC substrate utilized
- Significant thicknesses of the SiC layer can be obtained, up to several tens of μm
- The thickness control is limited by the grinding process
- Low-cost process

Technological difficulties and other drawbacks

- Plasma etching of thick SiC layers – utilizing hard metallic masks (Ni)

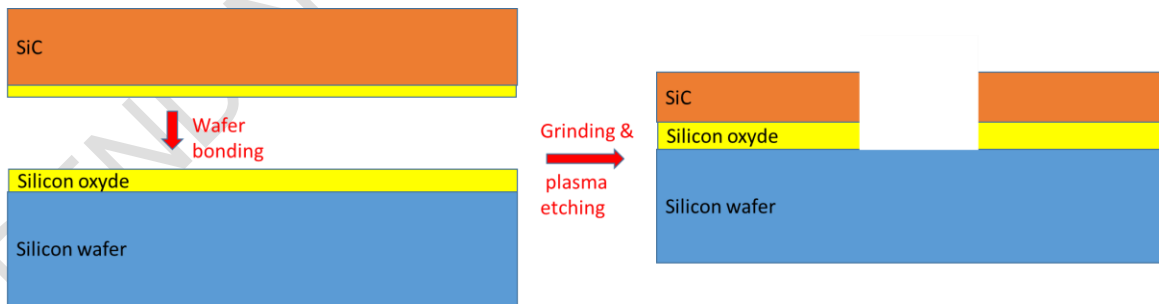


Figure 9. Process for the bonding SiC/Si structure

3.1.2 PECVD SiC/Si structure

Advantages:

- Low cost process
- The thicknesses of the layers are well controlled
- Etching process well controlled with Optical Emission Interferometry (OEI)

Technological difficulties and other drawbacks

- Amorphous SiC layers are obtained by PECVD. The conductivity should be controlled during the PECVD or by post-deposition activation annealing at high temperatures
- The thickness of the SiC layer is limited to several μm

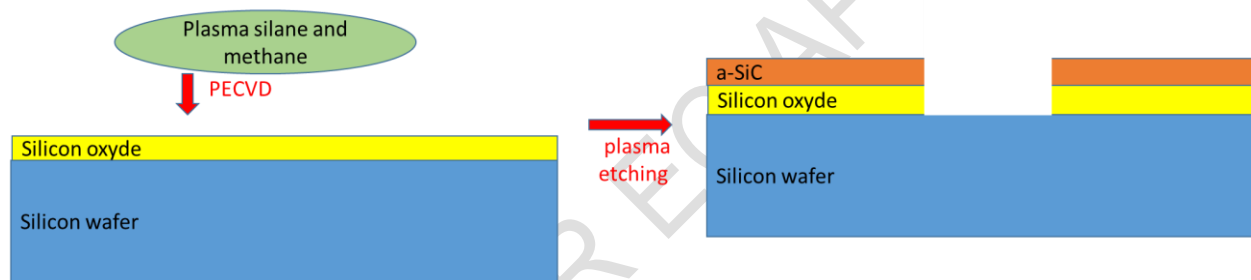


Figure 10. Process for the PECVD SiC/Si structure

3.1.3 All SiC structure

Advantages:

- Single-crystal quality with homo-junctions
- P/N junction isolation of the functional SiC layer in surface
- No silicon layers which will not resist to high electric field inside the structure
- No silicon oxide layer which can create interface problems and limiting high temperature annealing treatments (necessary during SiC fabrication process)
- The thicknesses of the layers are well controlled and thick N++ layers can be envisaged on the top
- Etching process well controlled

Technological difficulties and other drawbacks

- High cost of the epitaxial layers but structures already utilized during fabrication in our clean-room of SiC high voltage devices
- N++ layer on the top can be also created by ion implantation but to increase the layer thickness non-standard condition must be envisaged as high energy ion implantation or in canalization configuration (already studied for power devices)

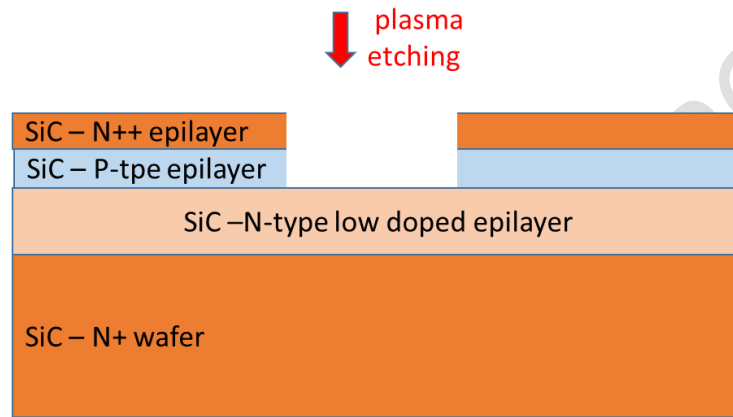


Figure 11. Process for the all SiC structure

3.2 First technological results

3.2.1 SiC to Si wafer bonding

The classical process utilized for Si-to-Si direct wafer bonding has been adapted to Si-to-SiC wafers. We exploited the fact that SiC wafers also exhibits a thermal oxide which is SiO_2 as for silicon. After a specific cleaning, high quality (TTV < 1 μm) oxidized Si wafer have been put in contact with SiC wafer using a SB8e bonder machine from SUSS-Microtec.

We tried bonding both Si and C faces of the SiC wafers. Only positive results were obtained on the Si-face of the SiC wafers. For these last ones, nice visual aspects are obtained (cf. **Figure 12**). Then, the bonded structure has been annealed under N_2 at 1050°C during one hour.

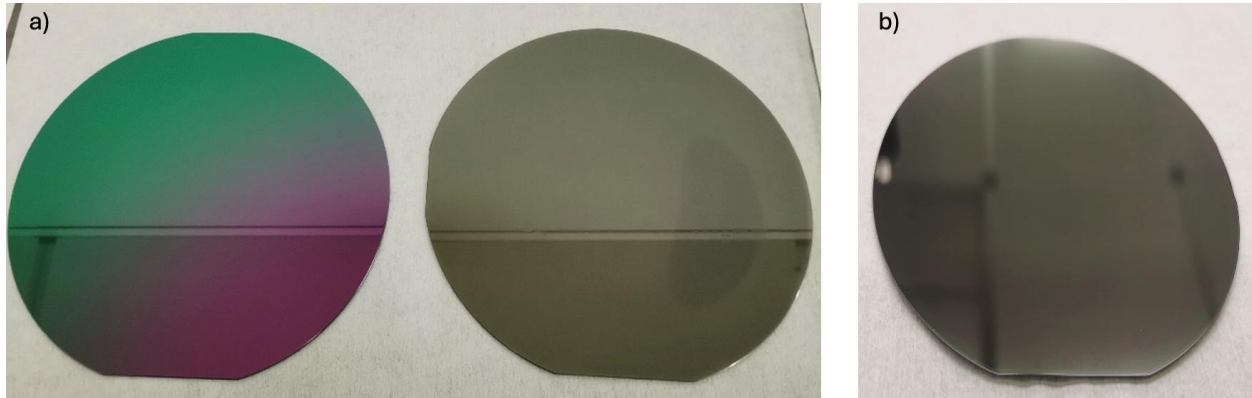


Figure 12. a) Photo of an oxidized Si wafer (left) and a SiC wafer (left). b) Bonded SiC/Si wafer.

However, a curvature measurement has shown a fial bowing of ~ 5.5 mm (**Figure 13**).

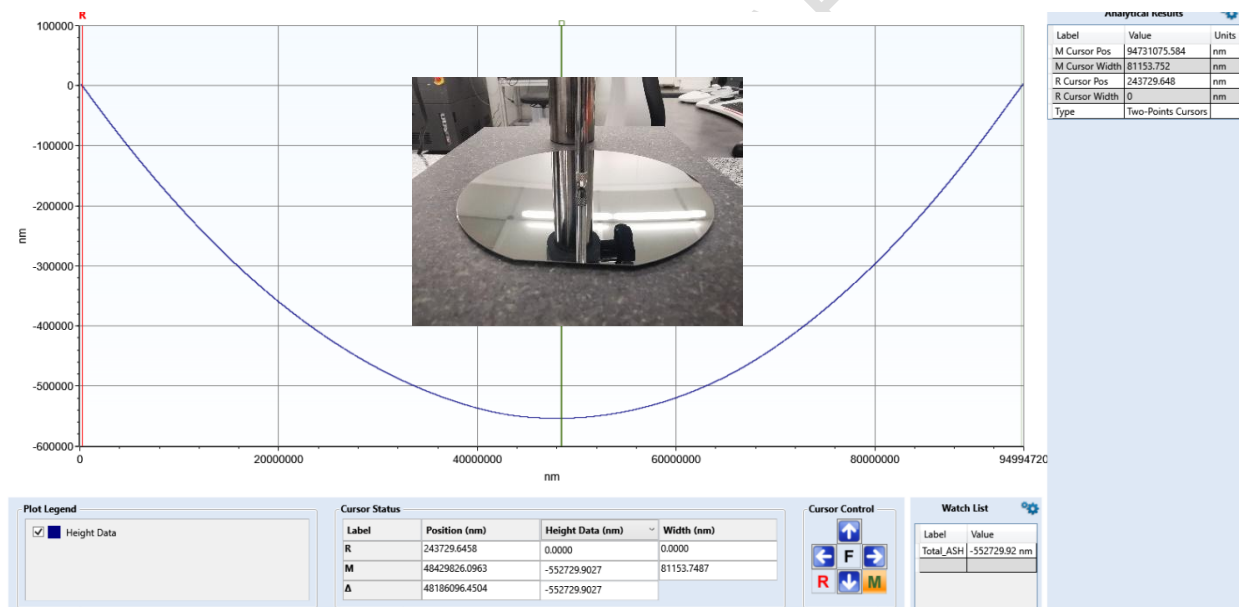


Figure 13. Si/SiC wafer fusion resulting in a bow of 5.5 mm.

We have validated the direct bonding of Si/SiC wafers and the associated sealing process. For future samples, the thickness of the SiC wafers will be reduced by grinding, a technological step already used in SiC technology for power electronics. Thinner SiC layers will reduce the stress on the structure. In addition, limiting the thickness of this layer to several tens of μm will facilitate the next step of opening it up by fluorinated plasma etching.

4 Conclusions

In this report, we presented the fabrication and testing of silicon-based plasma switches designed to operate between 350 V and 800 V. However, rapid degradation occurs in the switches, even for the one designed to operate at the lowest voltage. SEM images showed silicon melting due to the high temperature generated by the electric spark.

To address this issue, we proposed using SiC instead of silicon. This wide bandgap semiconductor can withstand electric fields ten times higher than silicon and extreme temperatures, which should prevent the micro-melting observed previously.

The use of SiC wafers for MEMS devices is a new approach that requires the development of new fabrication steps. Three processes have been proposed for the manufacture of the SiC plasma switch, and the first step of one of them has been validated. It consists of bonding a SiC wafer and a Si wafer. The next steps in this work will be to etch the SiC to obtain two electrically isolated electrodes, then to test the plasma switch at high voltages above 400 V.

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